Heterogeneous 3D Integration Technology and New 3D LSIs

Mitsumasa Koyanagi[1*], Kang-Wook Lee[1], Takafumi Fukushima[1] and Tetsu Tanaka[2]

[1] New Industry Creation Hatchery Center, Tohoku University, Sendai 980-8579, Japan
[2] Graduate School of Biomedical Engineering, Tohoku University, Sendai 980-8579, Japan
* Email: koyanagi@bmi.niche.tohoku.ac.jp

Abstract

A new 3-D integration technology and heterogeneous integration technology called a super-chip integration is described. A number of known good dies (KGDs) with different sizes and different devices are simultaneously aligned and bonded onto lower chips or wafer by a chip self-assembly method using the surface tension of liquid in the super-chip integration. Possibilities for new system-on-a chip and heterogeneous LSIs by 3D super-chip integration such as 3D stacked multicore processor with self-test and self-repair function, GPU stacked 3D image sensor with extremely fast processing speed and 3D stacked reconfigurable processor with spin memory are discussed.

1. Introduction

Various concerns have emerged in LSIs as the device size is scaled down to less than a few tens of nanometer. Three-dimensional (3D) integration technologies using through-Si vias (TSVs) are going to be employed in all kinds of LSIs to mitigate these concerns. We had proposed 3D integration technology based on wafer-to-wafer bonding method in 1989 and fabricated several 3D LSI prototype chips such as3D image sensor chip (IEDM, 1999), 3D shared memory (IEDM, 2000), 3D artificial retina chip (ISSCC, 2001) and 3D microprocessor chip (IEEE Cool Chips, 2001) [1]-[7]. So far the wafer-to-wafer 3D integration technology and the chip-to-wafer 3D integration technology have been developed. However, the wafer-to-wafer 3D integration technology has a serious problem that the overall chip yield exponentially decreases with an increase in the number of stacked layers. On the other hand, the inherent problem in the chip-to-wafer 3D integration technology is the low production throughput. To solve these problems, we have proposed a new 3D heterogeneous integration technology called a super-chip technology [8].

2. 3D Integration and Super-chip

The cross-sectional structure of the 3D LSI with TSVs is illustrated in Fig.1. The thinned upper layers are stacked onto the thick LSI wafer in a 3D integration technology based on a wafer-to-wafer bonding. In these 3D LSIs, a relatively thick Si substrate remains after completing the fabrication process. This remaining Si substrate is useful for reducing the mechanical damage caused to the devices during the 3D fabrication process. The electrical interconnection in the vertical direction is created by the TSVs and the metal micro bumps. TSVs are fabricated before the transistor formation in a via-first process whereas those are fabricated after the transistor formation in a via-middle process. Furthermore, TSVs are fabricated after completing the BEOL of CMOS process in a via-last process. There are two kinds of via-last processes of the front-via process and back-via process. We had initially developed a 3D integration technology with the via-first process using poly-Si TSVs and fabricated several prototype 3D LSI test chips of a 3D stacked image sensor chip, 3D stacked memory, 3D stacked artificial retina chip and 3D stacked microprocessor chip. Subsequently we developed the tungsten (W) TSV and copper (Cu) TSV technologies with small diameter to reduce the TSV capacitance as shown in Fig.2.

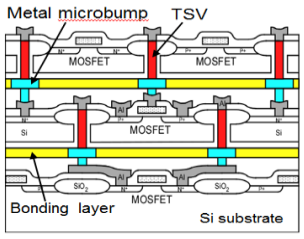


Fig.1 Cross-sectional structure of 3D LSI with TSVs.

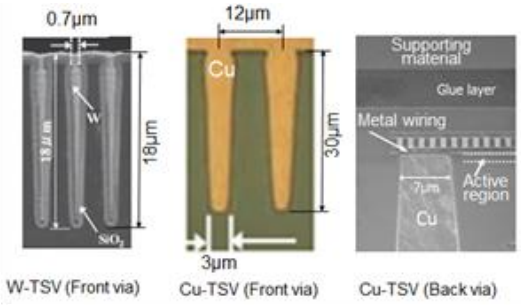


Fig.2 Cross-sectional micrograph of three kinds of TSVs.

We have also developed a new 3D integration technology using multichip-to-wafer bonding to achieve a 3D super chip as shown in Fig.3. A chip-to-wafer bonding is required to stack known good dies (KGDs) or LSI chips with different sizes and different technologies. However the fabrication throughput is very low in the

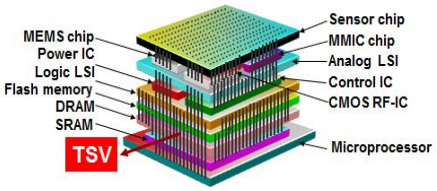


Fig.3 Structure of 3D super-chip.

conventional chip-to-wafer bonding method since chips are sequentially picked up and placed onto a wafer. Then we proposed a new multichip-to-wafer bonding method as shown in Fig.4 in which many KGDs or chips with different sizes and different technologies more than several hundreds or several thousands are simultaneously aligned and bonded onto a wafer. We have developed a new self-assembly technique using the surface tension of liquid for our multichip-to-wafer bonding method as shown in Fig.5. We have developed a self-assembly

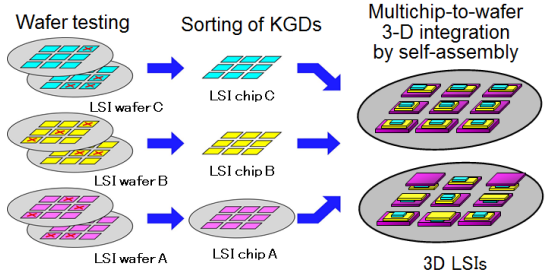


Fig.4 Super-chip fabrication by multichip-to-wafer bonding.

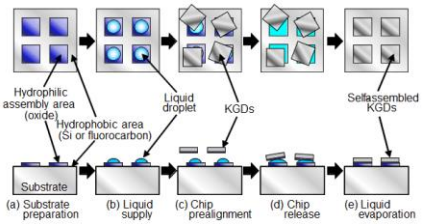
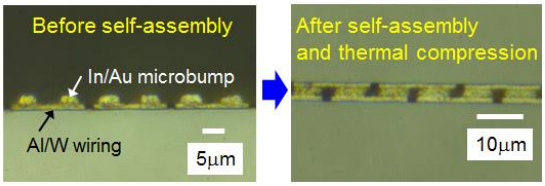


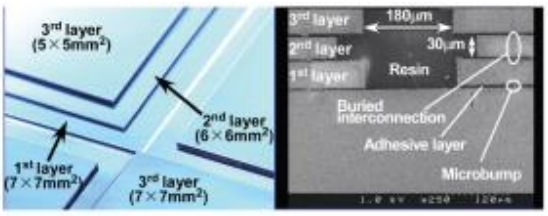
Fig.5 Self-assembly technique using the surface tension of liquid.

machine for 8 inch wafer. We simultaneously aligned and bonded more than five hundreds of KGDs onto an 8 inch wafer using this machine. The total alignment time was less than 1 sec. and the average alignment accuracy was 0.5μm. Fig.6 shows the cross-sectional view of



(a) (b)

Fig.6 Photomicrograph of cross-sectional view of stacked dies with In/Au microbumps fabricated using self-assembly.



(a) (b)

Fig.7 Photomicrograph of plan view (a) and SEM micrograph of cross-sectional view (b) of 3D test chips with different chip sizes.

upper and lower dies with In/Au microbumps stacked by the self-assembly. The size and pitch of microbump are 5μm and 10μm, respectively. We have also fabricated 3D LSI test chips by the super-chip integration technology using the self-assembly technique. Fig.7 shows photographs after stacking three layers of KGDs with different size onto a thick LSI wafer. A MEMS chip was stacked on an LSI chip using the self-assembly technique in Fig.8 where the LSI chip was bonded to the silicon substrate also using the self-assembly technique and Cu wirings were directly formed onto this chip and the substrate.

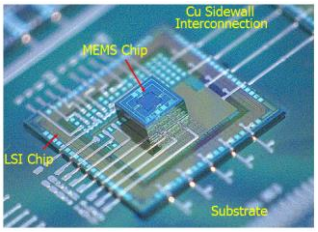


Fig.8 Vertically stacked MEMS chip on LSI chip by self-assembly.

3. New 3D LSIs and Systems

We can create various kinds of new system-on-a chip (SoC) with parallel processing and parallel data transferring capabilities by employing 3D stacked structures having many TSV's. Typical example of new 3D SoC's is a 3D-stacked image processor chip as shown in Fig.9 where image sensor chip, ADC chip, image processor chip and memory chips are vertically stacked. Several thousands of ADC's simultaneously operate in parallel to achieve an extremely high data conversion rate and high frame rate of more than 10,000 frames/s for image processing in this 3D-stacked chip. We have designed and fabricated a 3D-stacked image sensor test chip for this 3D-stacked image processor as shown in Fig.10. A highly dependable multicore processor with 3D-stacked structure as shown in Fig.11 is another example of new 3D-SoC's where a self-repair and redundancy circuit layer and a test circuit layer with BIST and scan path circuits are inserted between a processor chip and memory chips. In this 3D multicore processor, real-time testing is performed in the test circuit layer and failure circuits are replaced by self-repair and redundant circuits in the self-repair redundancy circuit layer to achieve a higher dependability. We have designed and fabricated a 3D test

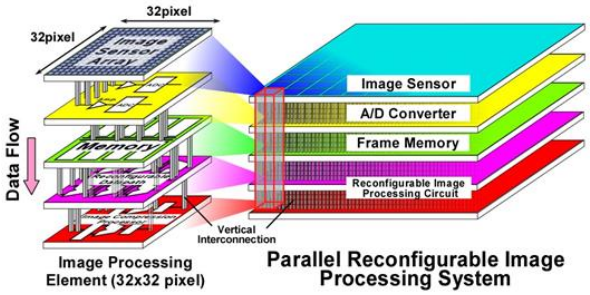


Fig.9 Configuration of 3D-satcked image processor.

chip for this dependable multicore processor as shown in Fig.12. Fig.13 shows a 3D reconfigurable processor with spin memory (SPRAM) where reconfigurable spin logic chips are stacked on a multicore processor chip [9]. Circuit configureation is changed by configuration

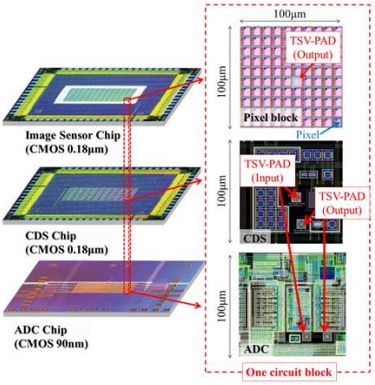


Fig.10 Fabricated 3D-stacked Image sensor test chip.

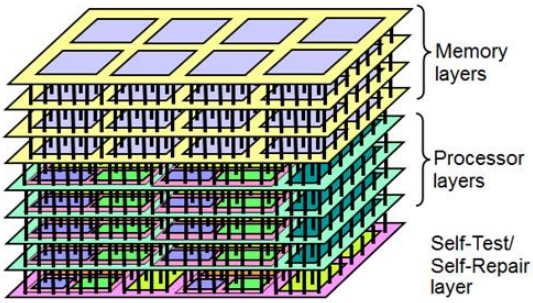


Fig.11 Configuration of highly dependable 3D multicore processor with self-test and self-repair function.

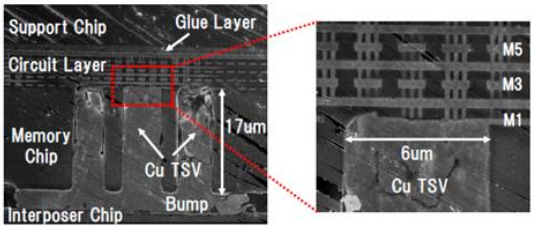


Fig.12 Fabricated 3D test chip for dependable multicore processor

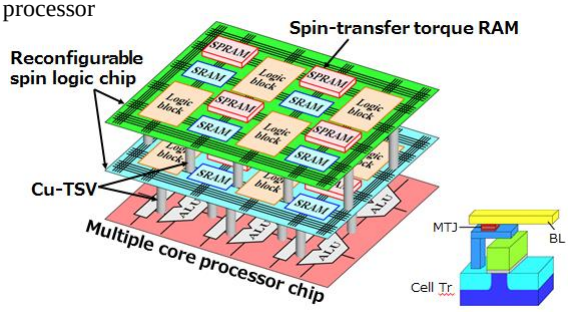


Fig.13 3D reconfigurable processor with spin memory (SPRAM).

data of spin memory. A 3D reconfigurable processor test chip with spin memory was designed and fabricated as shown in Fig.14. Magnetic material of MTJ (Magnetic Tunnel Junction) which is the key device for SPRAM is not tolerant to high temperature process for 3D stacking. Then we have developed a relatively low temperature

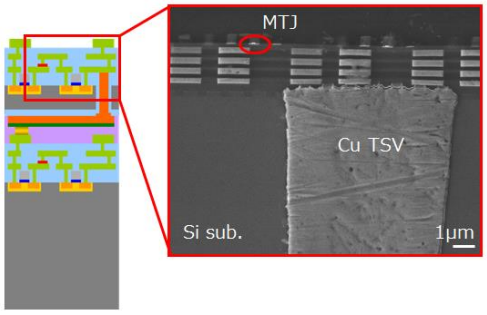


Fig.14 SEM cross-sectional view of fabricated 3D reconfigurable processor test chip with spin memory.

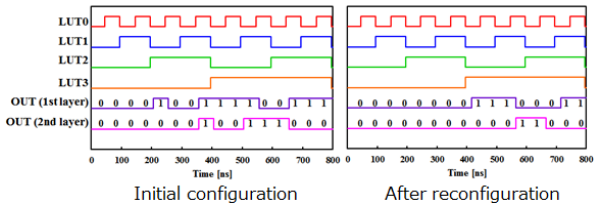


Fig.15 Waveforms of high speed parallel reconfiguration operation in the fabricated 3D-stacked reconfigurable spin logic chips.

process for 3D stacking of SPRAM using In/Au microbumps. Fig.15 shows a high speed parallel reconfiguration operation in the 3D-stacked reconfigurable spin logic chips. It is obvious in the figure that output data for circuit reconfiguration are successfully updated by data in SRAM working memory which are rewritten by SPRAM.

We have also proposed a new 3D hybrid integrated system as shown in Fig.16 where 3D SoCs, MEMS and photonic devices are integrated on an intelligent silicon interposer with optical interconnection and micro fluidic channels [10]. Fig.17 shows a photomicrograph of silicon interposer with optical waveguide, buried VCEL and buried photodiode. Fig.18 shows 3D photonic LSI where TSV (Through-Si Via) and TSPV (Through-Si Photonic Via) are used for vertical data transfer [11]. We have evaluated basic function of these 3D hybrid integrated system and LSI.

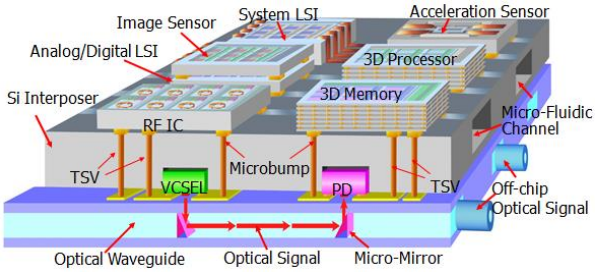


Fig.16 Configuration of new 3D hybrid integrated system.

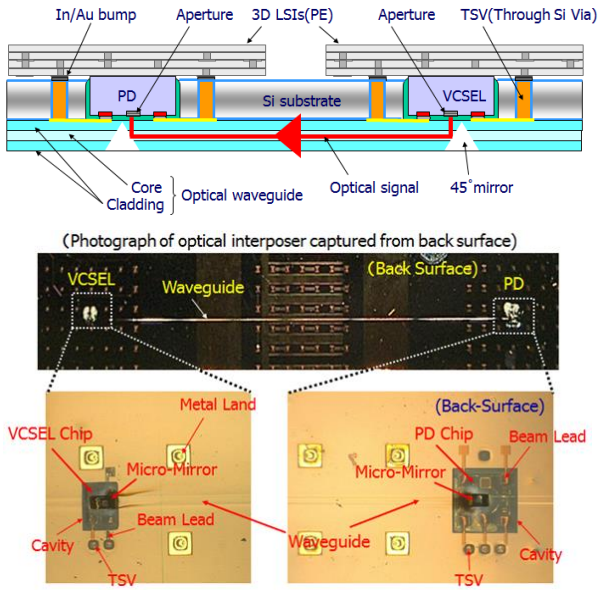


Fig.17 Photomicrograph of fabricated silicon interposer with optical waveguide, buried VCEL and buried photodiode.

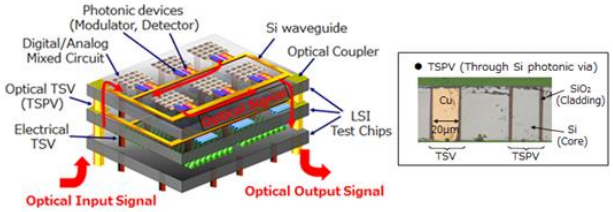


Fig.18 3D photonic LSI with TSV (Through-Si Via) and TSPV (Through-Si Photonic Via) for vertical data transfer.

4. Summary

We have developed a new 3D integration technology called a super-chip integration to achieve low-power and high-performance system-on-a chip (SoC). A number of known good dies (KGDs) are simultaneously aligned and bonded onto lower chips or wafers with high alignment accuracy by a new self-assembly technique using a surface tension of liquid droplets in the super-chip technology. We have proposed and described new 3D-SoCs with parallel processing and parallel data transferring capabilities such as a 3D-stacked image processor chip, a dependable multicore processor with 3D-stacked structure, a 3D reconfigurable processor with spin memory (SPRAM) and a 3D hybrid integrated system.

Acknowledgments

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